Proposal for a Shift Register Approach to RPC Calorimeter Readout for Test Beam, Cosmics, and Sources

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Abstract

Resistive Plate Chambers for Hadronic Particle-Flow calorimetry will have a large number of pixels. We present tests of a system for readout with parallel vertical shift registers, somewhat like that used in CCD imaging. In our case we discriminate on the signal immediately after amplification and shaping, and only shift single bits. We discuss the issues involved in a particular model for using off-the-shelf commercial chips for readout on a moderate scale. We have a 32 channel prototype in operation on an RPC, and we describe tests with the amplifiers etc leading up to this. The prototype is an example of a layout for the chips to be mounted on the readout pad for an RPC to make a thin assembly. Comparisons to other systems are made for cost scaling, modes of operation, etc. This particular implementation uses analog delay instead of a digital pipeline, and has no clock on the board during detector live time. This RPC readout system could be implemented quickly. Production of this system should have minimal start-up costs and minimal start-up times. One advantage of the present system would be to provide readout of large numbers of channels on a short development time scale at low cost. This would allow initial tuning of the reconstruction and analysis software in a test beam before other readout systems are ready. It also provides risk management by development of another technology at small additional cost.

OUTLINE

INTRODUCTION

A new method of calorimetry, particle flow, has been studied primarily in Monte-Carlo, and to a limited extent in experiments. The method involves measuring the momenta of charged particles with tracking, for better resolution. In order to fully exploit this kind of calorimetry for even higher resolution, showers from the charged particles must be removed by tracking inside the calorimeter in order to measure the energy from neutrals such as neutrons and K-longs. One implementation of this would use Digital Calorimetry, in which only pixel hits are recorded, not analog/adc values. An Implementation of Digital Calorimetry that has been proposed uses Resistive Plate Chambers (RPC). Measurements of single planes of such chambers having up to 64 pads/pixels of 1 cm sq have been made using cosmic rays and sources. What is needed is a system of amplifiers and digital readout for many more channels. A small calorimeter in a test beam could be built with anything from 20 thousand channels to 400 thousand channels. This is system is needed both to study digital Calorimetry, and to gain understanding of hadronic showers in general.

The basic problem with Digital Hadron Calorimetry which involves internal tracking is the need to read out large numbers of channels, perhaps 4 x 10^5 channels in a test beam, and 10^7 in a real detector. Some people are approaching this problem by developing ASICs of eg. 64 channels which would be near each 8x8 set of pixels of each RPC, on the readout board in the calorimeter gap. One motivation for our alternative shift register approach was to avoid the high costs and long lead times of ASIC development, particularly for a test beam test in the near future. By using discrete commercial components we came up with a working prototype system which was put into operation quickly, with about a factor of 100 smaller startup costs. Cost estimates now show that this system is cost competitive with the ASIC approach for up to around 4 x 10^5 channels.

OVERVIEW

Devices with large numbers of pixels, such as digital cameras, almost invariably use the method of parallel shift registers to get the data out. Each row of pixels is shifted to the edge of the device, all rows shifting in parallel. At the edge of the device there can be orthogonal shift registers or other data processing. For digital calorimetery there is a significant simplification because we do not need the analog information. In general, one needs to amplify the signals, set a digital bit if the signal is large enough, and read out all the bits for 1 event.

The proposed system has amplifiers, comparators, and digital latch/shift registers on the PC boards of the RPC readout pad planes. This will fit in between the steel plates of a sampling calorimeter, along with the RPC active medium. Delay of the signal until the beam trigger arrives is accomplished in an analog way by using very slow amplifiers, not pipelines. This delay provides the optimum mode of operation for use in a test beam.

There is no digital clock on the planes during the live time, only after an event during the readout. It appears that the lack of clock noise will allow use of much simplified PC boards, compared to an ASIC system. The outputs of the comparators are latched into parallel-to-serial shift registers. The first stage of readout involves shifting out the bits from a number of cascaded shift registers to a microcontroller For the next stage of readout the microcontrollers have 8 bit wide tri-state outputs to a bus. Numbers of elements and timing considerations are given later. There is also a description of possibilities for the rest of the readout chain. The system should operate at hundreds of HZ.

The layout of surface mount parts on the top of the PC board for one channel takes up the same area as a pad on the bottom, on average. The layout is that of an infinitely extensible grid. There are practical limits on the size of one readout board, roughly 1 meter, due to loads on logic signals. In any case, the limits on RPC size are about 1 meter, and PC boards of 1/3 meter may have to be spliced to get to 1 meter. In the present implementation the pads on the board are 1.1 cm square for the first prototype, and 1.2 cm for the second prototype.

If the RPCs are operated in avalanche mode, amplifiers are needed to get from 50 femto-Coulombs to discriminator thresholds of tens of milli-volts, with impedance to drive a comparator. There is a broad range of signal charges, but a threshold of roughly 50 femto-Coulombs is needed for full efficiency.

We have considered three implementations, which are related to different modes of operation:

1) One can use amplifiers with very high input impedance, and slow response. The signals from the pads at the amplifier input have fall times of many microseconds (although the rise time is still fast). The amplifier output can have a slower rise time, and is a high level for several microseconds. With this implementation, there is enough delay of the signal to allow for trigger formation in a test beam, and no other delay is needed. The signals can be latched up to a few microseconds after the event. If the latch is done with a parallel load of a shift register, the gate of the latch can be opened up to a microsecond after the trigger

2) One could use an amplifier with a low input impedance, and a fast response, and then use slow charge storage, either before or after the discriminator. In this case triggered mode could still be used.

3) One could use fast amplifier, discriminator, etc. The system could operate in cycling mode, and stop cycling when there is a trigger. We have typically used the CDF Rabbit system in this way for cosmic ray measurements.

We have implemented version number 1 because of the availability of 4 channel amplifiers which are extremely cheap, because of the ability to trigger with no clock on the board, and because there does not appear to be any problem with the very slow response.

In usual operation, a trigger signal from an external trigger on an individual beam particle arrives too late to open a gate for the signal of interest, so our analog delay of the signal is needed in order to latch the hits.
The system is relatively slow, in both analog and digital, but this doesn't matter for cosmic rays or low intensity test beams. It is a good match to the rate capabilities of the RPC detector itself.

There have been tests of each part of the system, leading up to several prototypes. After the first prototype was tested, Both the amplifier circuit and the Printed Circuit board layout were changed. Early tests included observations of analog pulses, characterization of amplifier bias and operation, efficiency tests with cosmic rays with both on-board and external discriminators, and readout of a multi-pad RPC into a laptop. Tests of the front-end chip on an RPC have worked well so far. Efficiency is essentially the same as with CDF Rabbit tests done previously. Looking at the outputs from multiple pads on a 4-trace scope also looks reasonable. There are a few potential problems, which are described.

A particular cheap system under consideration would have deadtime and could not handle beam rates over somewhere in the region of 100 Hz average, 500Hz instantaneous. However, this is a good match to the limits of the RPC itself, so it should not be a serious limitation. The overall operation of the first prototype described here was improved with a number of small changes in hardware and software. Actual reading speeds are described.

Specific proposal:
The system consists of standard ICs, available in both DIP and Surface mount. It works by reading out after an external trigger, as opposed to self-triggering,
There is enough delay in the system to use it in triggered mode.
Triggers on individual particles should be available to our system from test beams and with cosmics, and to some extent with sources.

The basic chain of electronics on the chambers is amplifier, comparator, parallel to serial shift registers. Immediately off the chamber are microcontrollers for readout and buffer memory.
The data from the microcontrollers can be combined and sent to a PC by a data collector.
A test of the amplifiers on an RPC gave pulses over 10 u sec wide. The readin time to the microcontrollers could be up to 1000 micro-sec for 100 pads. Each set of 100 channels would be read in parallel. More aspects of DAQ are described later.

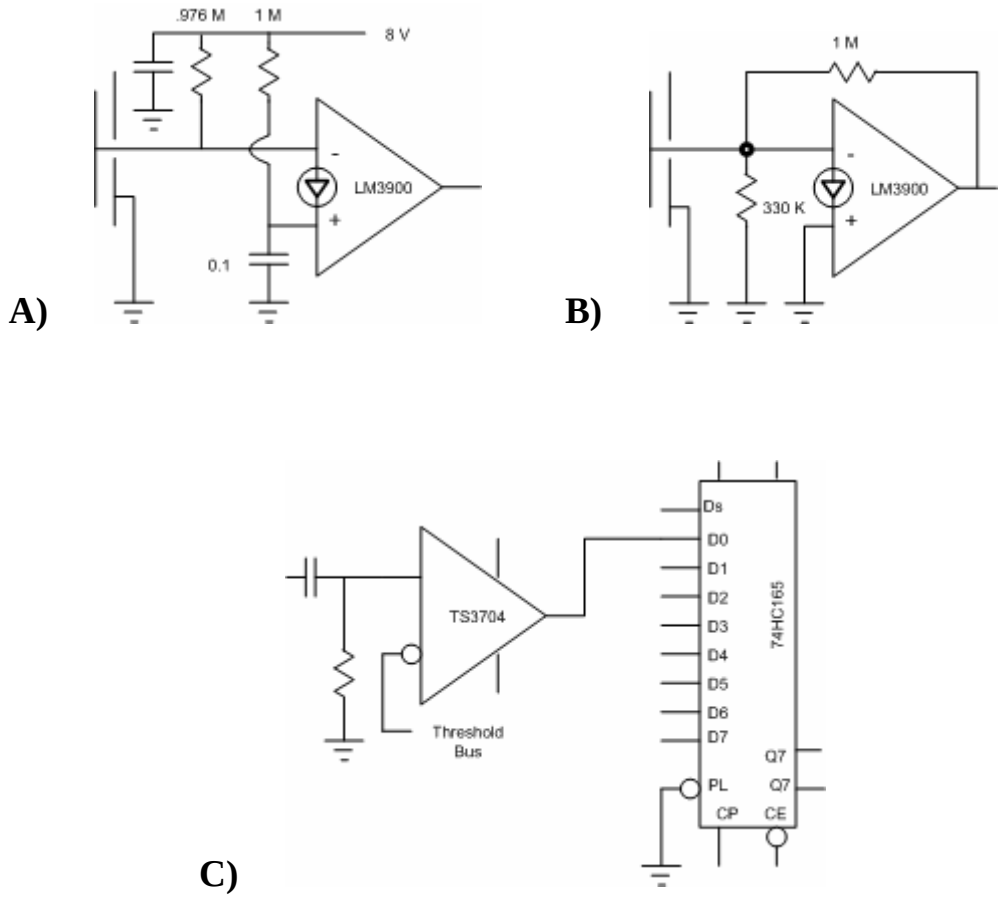


Fig. 1 Circuits used in the prototypes. A) For the first prototype the LM3900 current-to-voltage amplifier was run open loop with a small bias. B) For the second prototype feedback and self biasing was used. C) The rest of the basic cell circuit on the board: The TS3704 comparator is similar to an LM339 with internal pull-ups. The data is shifted off the chamber with a series of 74HC165 parallel-load shift registers. Figure 7 is a photograph of the circuit on the RPC.

TESTS

Many preliminary tests of the amplifier alone were done with a 2-gap RPC chamber using the new gas, 0.5% SF6, 5% Isobutane, and balance R-134A (Freon). Some tests were also done with a single gap chamber and a radioactive source.

In the first, and simplest test with an oscilloscope, Two signals were observed simultaneously on a scope, with the trigger on one of them. Many simultaneous signals of 50 mV and 10 u sec long (out of the slow amplifier) were seen. Occasional signals over 150 mV were seen, at a rate comparable to the scintillator telescope and the rate with very fast expensive amplifiers. (We used AD8015 or MAX3760? To see the actual fast signals from an RPC)

Efficiency Tests

Measurements of absolute efficiency were done using a single large readout pad (16 x 18 cm) and cosmic rays. Figure2 and Appendix C. Some measurements of relative efficiency were done with four pads of 1 cm sq and a radioactive source.

The basic result of these tests is that the efficiency is as good as was the case with an ADC system of 1 fC/tic, and using offline threshold cuts above pedestal.
A small correction was made for use of two different HV supplies, based on measurements with an electrostatic voltmeter.

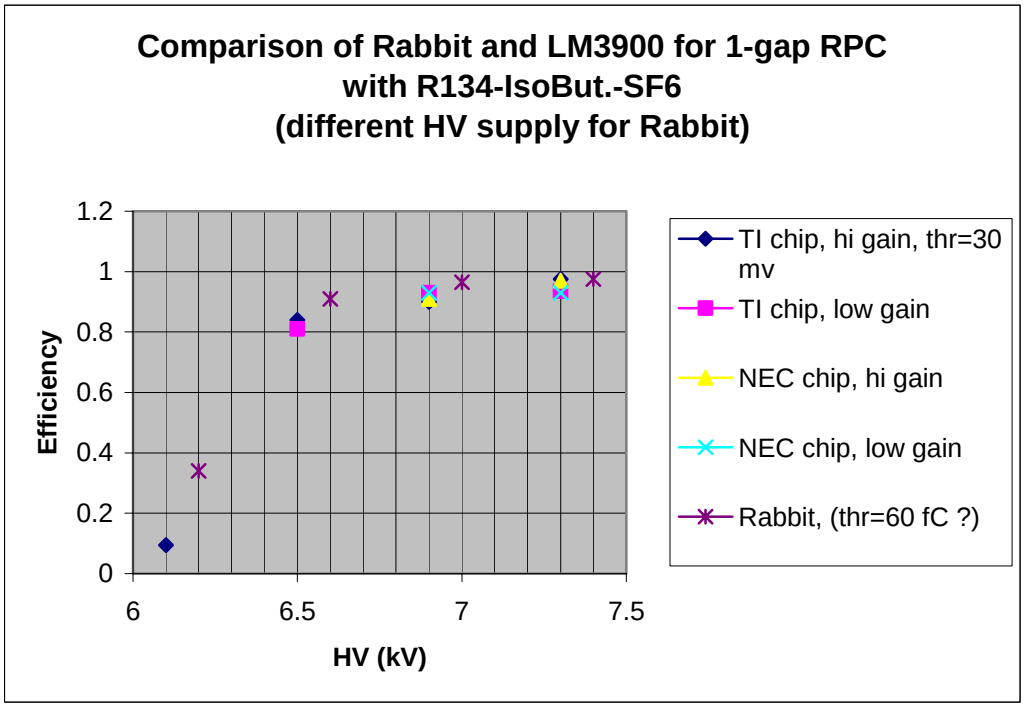


Fig. 2 Efficiency comparison for LM3900 amplifier A with an external discriminator vs a Rabbit ADC system of 1 fC/tic. A single large pad was used for the RPC in both cases. Efficiencies were measured with scalers. The efficiencies track very well.

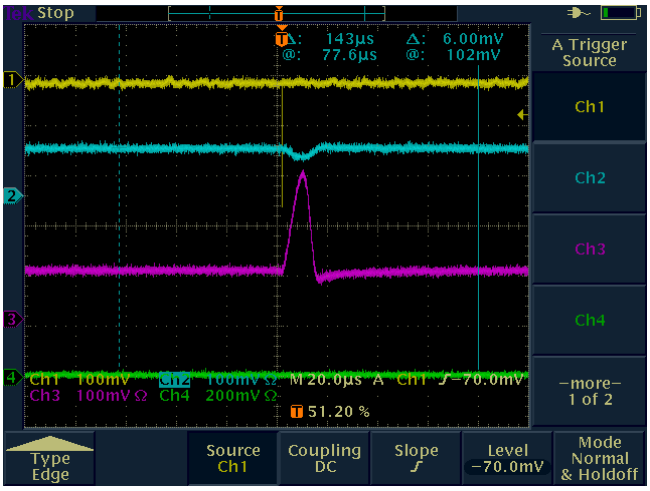


Fig. 3 RPC Signals out of LM3900. Ch 3 (pink, positive, about 200 mV) is from pad hit by signal from electron from beta source. Ch 2 (blue, negative) is from adjacent pad.

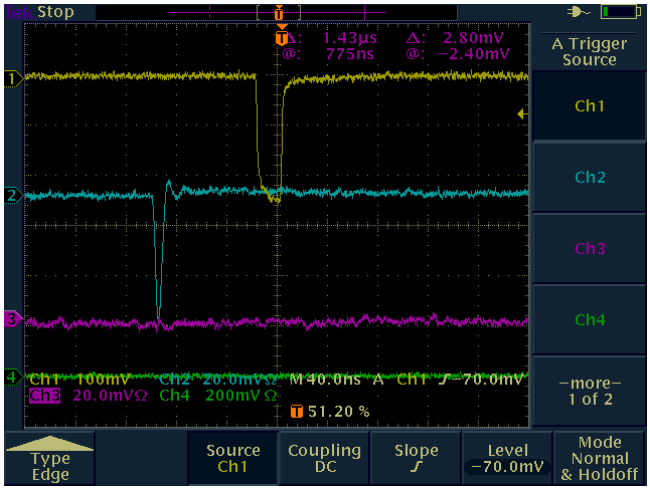


Fig. 4 RPC signal after a fast video amplifier. The shape is only slightly modified by the amplifier. Channel 2, blue, negative 50 mV and about 5 ns wide fwhm. Channel 1 is the attenuated discriminator output from the trigger scintillator.

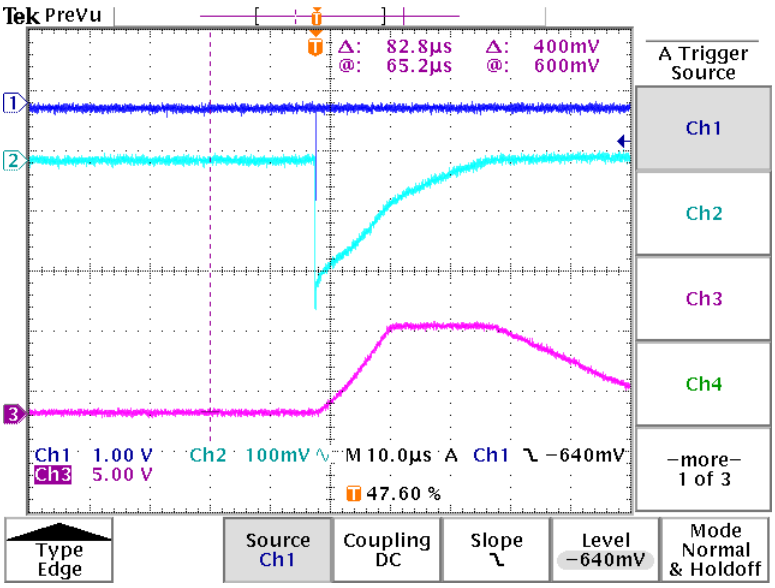
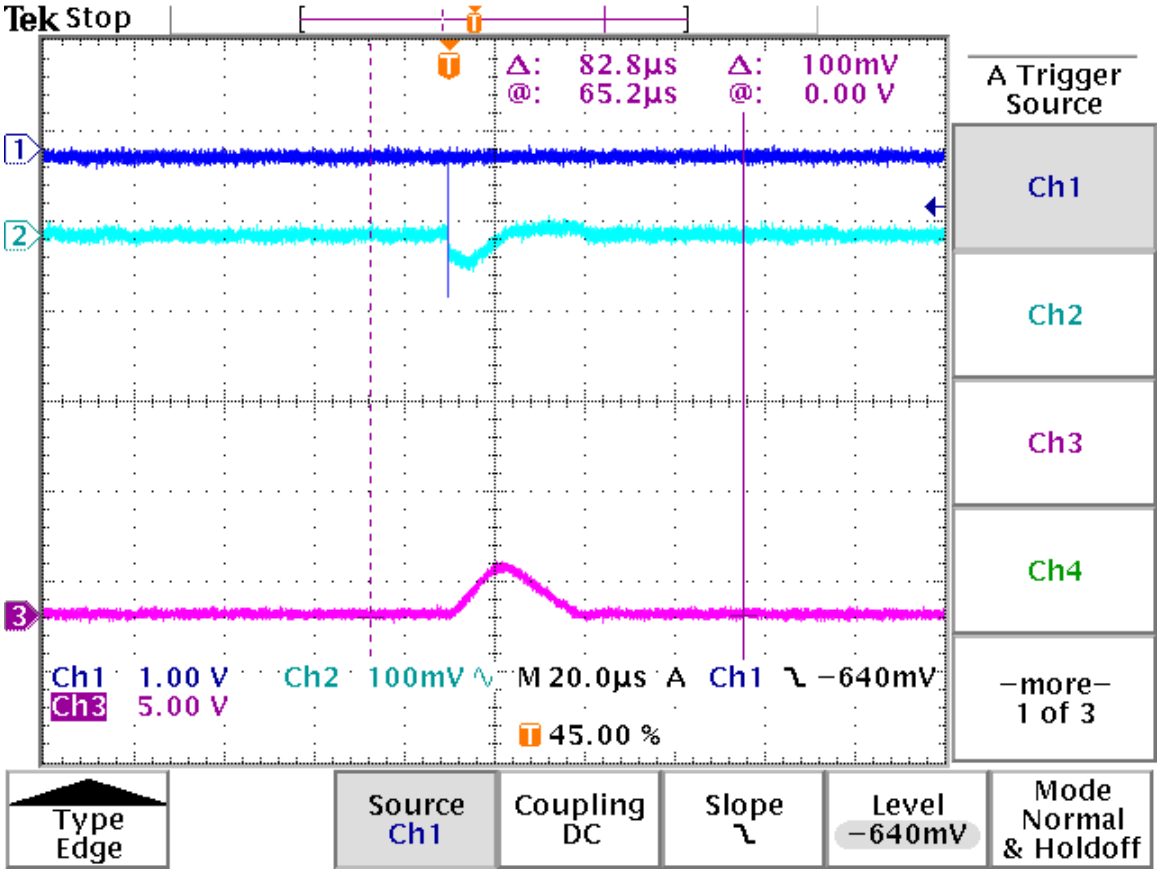


Fig 5a and b Signals into and out of LM3900 amplifier. Because of the high impedance input, the RC time constant with the particular 5x6 cm pad was around 10 u sec. We can see both the fast electron signal, and the slower accumulation of charge from the heavy ion drift at around 5 u sec. This example is a large signal, around 25 pC, probably a streamer. The 1.2 cm pads of the prototype system have much smaller capacitance than this.



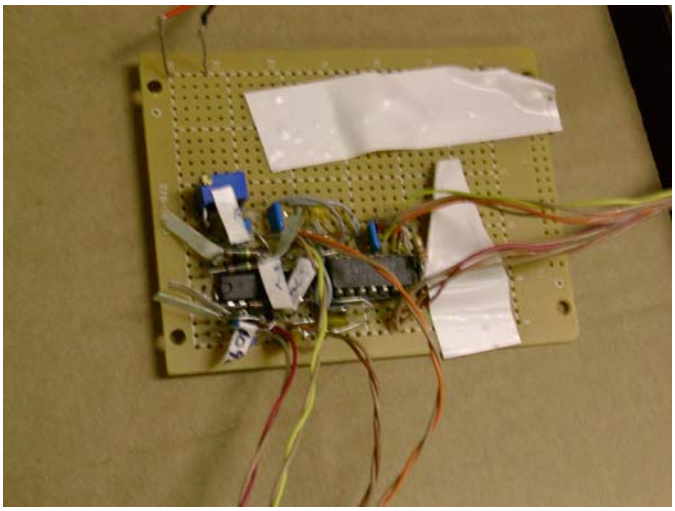


Fig. 6 Dip-Chip version of amplifier A and comparator used for tests.
This demonstrated the lack of feedback from the digital comparator output to the signal input in a breadboard version. This circuit was used for measuring the relative efficiency of a 4-pad area of RPC with a radioactive source and scintillator trigger.

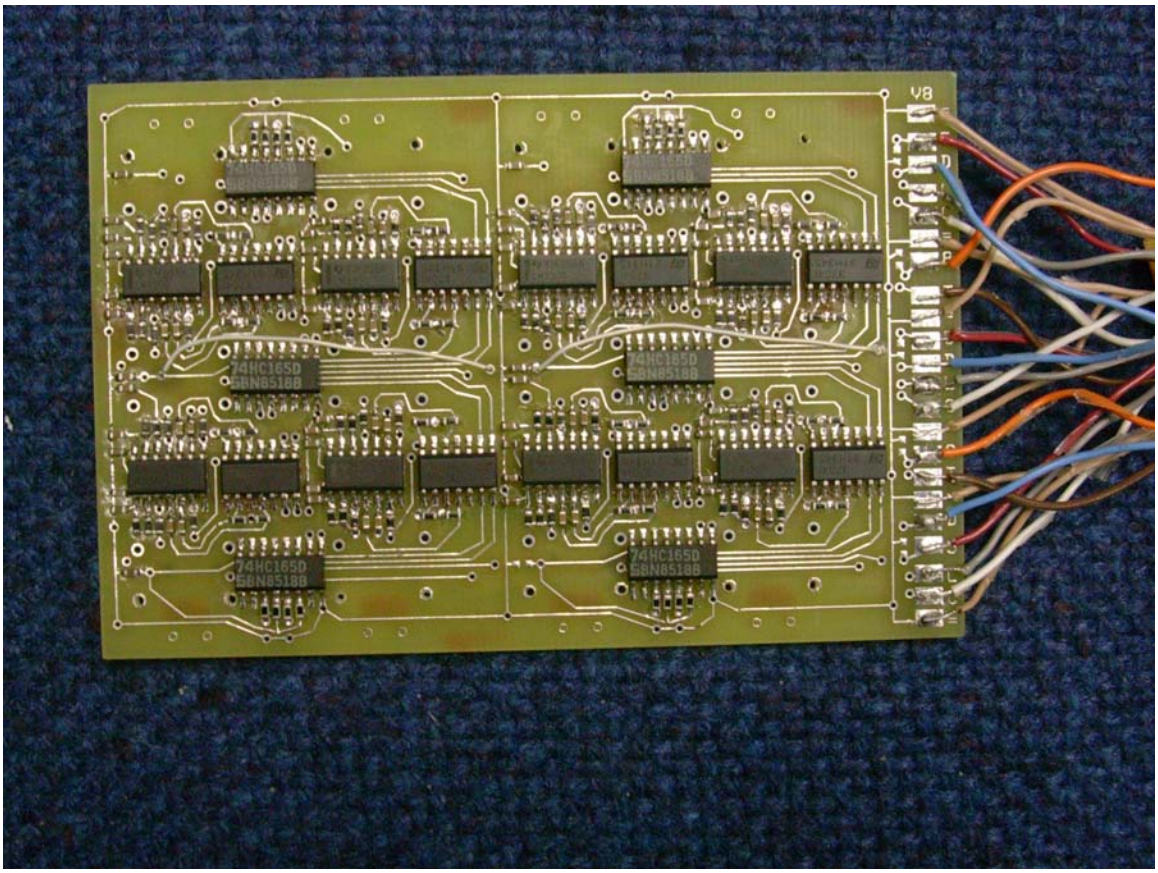


Fig. 7 The first 32 channel prototype, demonstrating layout of amplifier, comparator, and shift register readout to fit on the back of a padboard with 1.1 cm sq pads. This pattern can be repeated for a very large number of channels (eg 100 x 33). This board was designed for 32 channels. This was used to read out the RPC to a laptop.

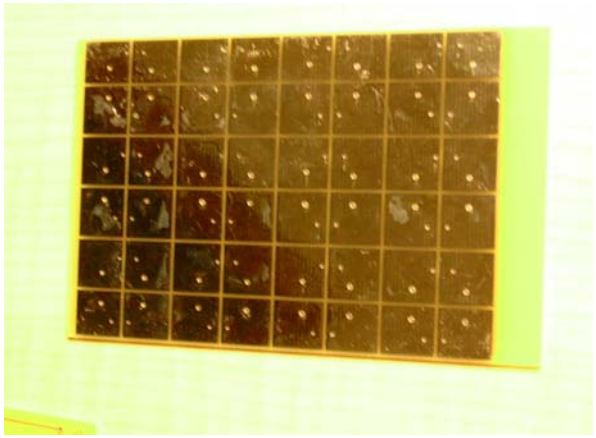


Fig. 8 The pad side of a board. These pads are 1.1 cm sq. The plated through holes for feeding signals to the upper layers are visible.

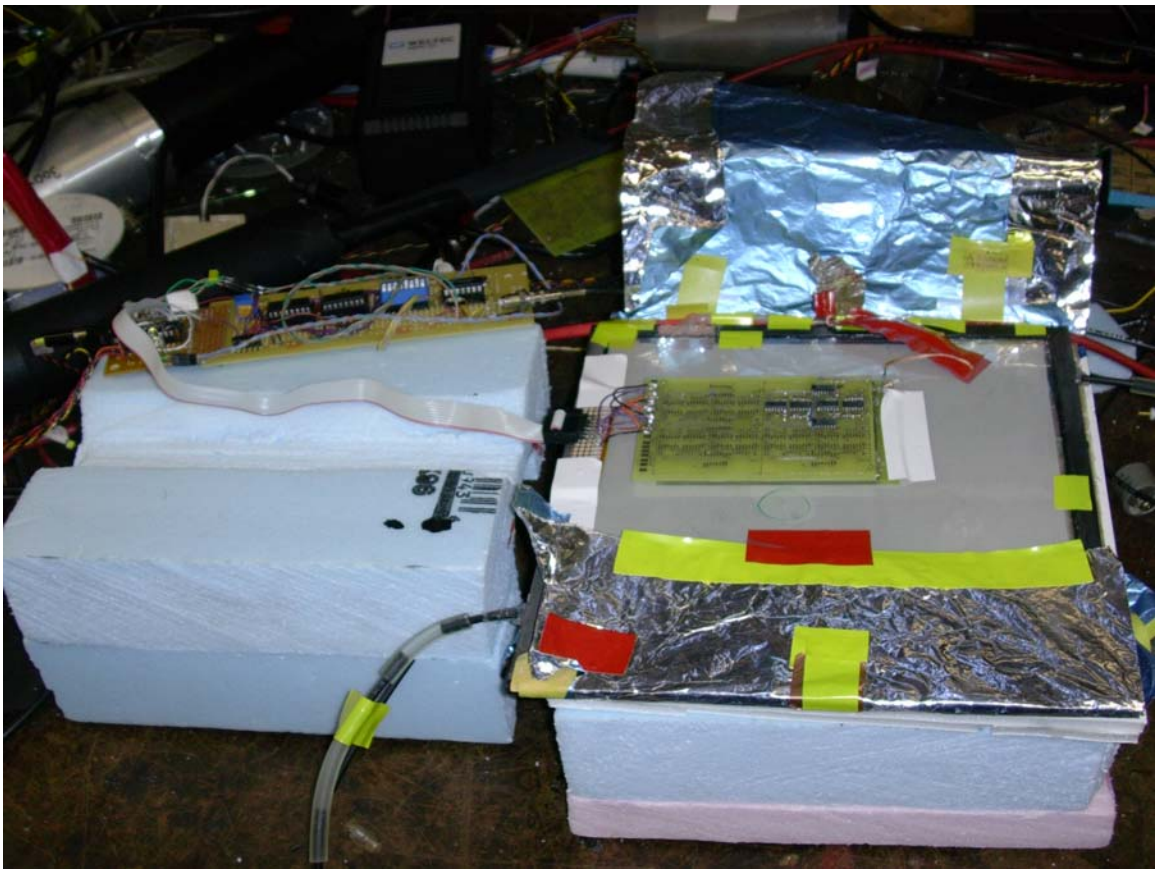


Fig. 10 Setup of prototype system to read the multi-pad RPC into a laptop. The board with pads and readout is on the surface of the RPC. It has chips installed for 8 pads. The microcontroller and associated trigger logic are to the left. In normal operation the RPC is shielded, and one of the trigger scintillators for cosmic rays is above it.

Description of Prototypes

This development was done as an iterative process. On the basis of testing prototypes, changes were made to the Amplifier circuit, PC board layout, DAQ software, trigger logic, offline software, etc. We describe the tests of the first few prototype systems, and improvements which were made.

For reasons of cost, the PC board on the RPC was implemented with two PC boards of 2 sides each rather than a 4 layer board with blind vias. One was the pad board and signal ground plane, the other was the board for the surface mount chips, and interconnections , signal lines, digital ground, and power. The ground planes of the two boards were connected with silver-loaded silicone. A possible issue for the future is whether a 4 layer board with blind vias is really needed, or if two simple, inexpensive boards can be connected so that there are adequate ground paths and signal returns between them.

Signals: For the original amplifier circuit A, the threshold of 15 mv appeared to correspond to around 60 fC RPC signal, with 5 to 8 V supply to the amplifier. Using charge injection, the gain of the amplifier B was measured to be about twice as high. It is interesting that the effective gain of the obsolete NEC version of the chip was another 50% higher, probably due to a change in input impedance.

In version A of the amplifier, the chip was run open loop, with bias supplied by using slightly different currents into the two inputs. This was not suitable for a system of many channels because the required difference in currents was different channel to channel. The bias must be adjusted so that the amplifier in on the high-gain portion of the output vs input curve.

In version B of the amplifier, the internal input-offset current was used to bias the amplifier to always be in the high gain region. Also, the use of the feedback resistor matches the channel gains.

The signal output from the amplifier was about 7 u sec wide with the NEC dip chips (no longer in production) (see Appendix C), and somewhat wider with the TI soic chips. In the first prototype with amplifier circuit A the signal was AC coupled to the comparator, because the channel-to-channel pedestal levels out of a chip varied by around 10 mV.

The gate initiated by external trigger was 5V CMOS, negative going, and 10 u sec wide. The interrupt to the uP was positive, 1 u sec wide.

The microcontroller readout and associated logic was implemented in DIP on prototyping boards. A PIC 16F84 20 MHz was used because the programmer for it was available. The software development was done in the C language.
The additional logic included two FF / timers used to generate delay and also the load gates for the shift registers, and to provide an interrupt to the uP after the gate. Both Q and Q-bar are needed. Also, two 74hc164 chips with known inputs and switch settable inputs were provided for testing the readout and software development without the RPC. The software used fixed pin IO directions to make it much faster.
The data output was changed from ascii hex to binary to make it much faster. The offline serial program was changed to display in hex for debugging.
Other improvements could be made to this system:
1) The software should disable interrupts during the serial output to the laptop, and provide a busy signal.
2) The uP busy and a fast logic busy should be ORed together to block triggers.
3) The serial output is only for prototype testing and for a larger system would be replaced by byte-wide tri-state outputs.

Results of Tests of First and Second 32 Channel Prototypes

There were a number of problems with uniformity of response in the first prototype which used amplifier A, and the early PC board layout. These problems were eliminated in the second prototype which had amplifier B and a new PCB layout.

The overall 4 layer PC boards were made up of two boards of 2 layers, with only minimal connection between the two grounds (analog signal and digital signal) of the two boards. In early versions of the board the ground traces on the top board were very narrow. There was not enough room on the board for all the power leads to both analog and digital parts of the circuit, so external wiring was used. With a pad grid of 0.425 inch (1.08 cm) there was not room for ground traces to isolate the amplifier inputs from the digital signals. The second prototype has pads of 0.475 inch (1.20 cm) and has room for power traces, good grounds, etc.

Response was measured by number of hits in each pad with roughly uniform coverage by the cosmic ray trigger setup. Most of the original problems were due to problems with the Printed Circuit board layout and construction. This was for the 32 channel prototype labeled V8. The layout was the problem for 4 "hot" and probably for another 7 "cold" channels of the 32. There were another 3 cases where non-uniformity could be correlated with non-uniformity of the amplifier gain measured dc. Thus roughly half the channels were clearly affected in some way.

These results led to the Revision of both the PC board layout, and the amplifier circuit for the second prototype.

PAD NUMBERING SCHEME:

2x	2x	2x	2x	0x	0x	0x	0x
3D	3C	3B	3A	1D	1C	1B	1A
6D	6C	6B	6A	4D	4C	4B	4A
7D	7C	7B	7A	5D	5C	5B	5A
10D	10C	10B	10A	8D	8C	8B	8A
11x	11x	11x	11x	9x	9x	9x	9x

In the first version, hot channels 3C, 1C, 7C, 5C were hit almost every event because the RPC pad line to the LM3900 amplifier was not isolated from the load line of the adjacent 74HC165 register. The analog amplifier picked up the digital load signal to the extent that the comparator was triggered.

Cold channels were found at the bottom right of the LM3900 in 7 of 8 possible cases. Possibly the ground pin of the LM3900 did not have a low enough impedance path to ground, and the analog ground was intermixed with the digital ground.

The gain-setting resistors for amplifier A were measured both before and after construction of the board. The non-uniformity of gains of some amplifier channels is probably due to non-uniformities in the chips. The DC gain was determined from the

quiescent level of the output of a channel. This had been correlated with gain in extensive previous studies of the chip.

```
N-hits, by geometric location
      0    935      0    934      1    934      0    934
     22     50     81     84     86     79     78     65
     53     99    127    125    134    139    130     98
     71    108    142    160    155    139    122    105
     67    112    128    133    120    113     98     71
      0    935      0    935      0    934      0    934


N-hits, by geometric location
      0      0      0      0      0      0      0      0
     22     50     81     84     86     79     78     65
     53     99    127    125    134    139    130     98
     71    108    142    160    155    139    122    105
     67    112    128    133    120    113     98     71
      0      0      0      0      0      0      0      0

nevt, nonzevt       935     745
effic 0.796791
ave no hits 3.927273
```

Table A The Pad Hit populations for prototype #2 reflect the acceptance of the cosmic ray trigger as expected, and do not show any problems.

```
N-hits,  No cuts,  by geometric location
      0   2338      0   2338      4   2335      4   2336
    161   2103    298    381   2173   2196    234     42
     73     70     99     40    232     31    151    116
    222   2151    176    144    231   2308    207    124
    189     54     87     24    133     70     68     13
      0   2338      0   2338      0   2338      0   2338


N-hits, Filtered, by geometric location
      0      0      0      0      0      0      0      0
    161      0    298    381      0      0    234     42
     73     70     99     40    232     31    151    116
    222      0    176    144    231      0    207    124
    189     54     87     24    133     70     68     13
      0      0      0      0      0      0      0      0

nevt, nonzevt      2339    1871
effic 0.799914
ave no hits 1.581873
```

Table B Showing problems in the first prototype. Numbers of hits from each pad from a cosmic ray run with the first 32 pad prototype which used amplifier A and a compromised PCB layout. The run parameters were: threshold = 10 mV, delay before latch = 5 u sec, latch width < 1 u sec, RPC Voltage=7200. The second and fourth rows have hot channels in locations 2 and 6 (from the left). These channels are hot because the

amplifier input was in close proximity to the trace for the digital load. The top and bottom rows of the top table have the hard-wired inputs to the shift registers at the edge of the RPC. These are used for debugging. Other aspects are described in the text.

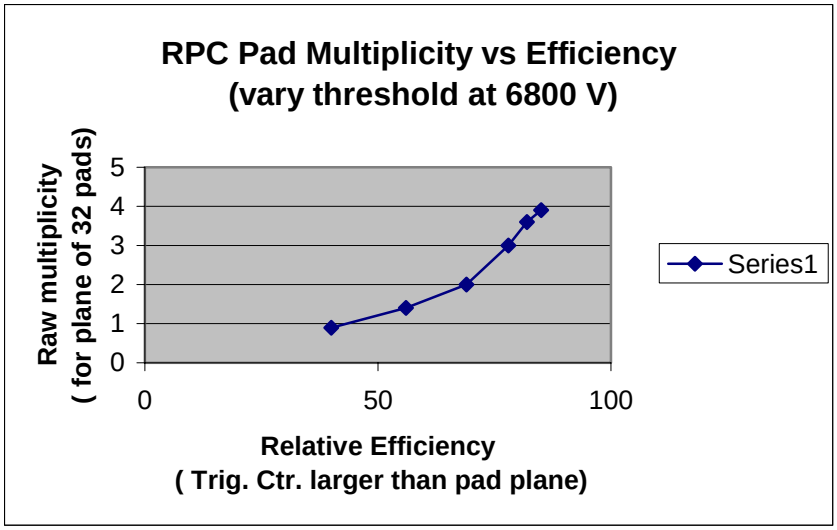


Fig. 10 Uncorrected measurement of RPC Pad Multiplicity vs Relative Efficiency. This was obtained by varying the comparator threshold with a fixed RPC voltage of 6800 Volts. The threshold was varied from 25 to 120 mV. Because the cosmic ray trigger counters are larger than the instrumented pad plane, there are false increases in efficiency from crosstalk (at large multiplicity) from uninstrumented pads which are inside the trigger acceptance and near the instrumented pads. A correction algorithm is being developed.

Software used for the Prototype includes:
CCS PIC C Compiler for programming board readin and serial out
PIC84 Chip Programmer
SimpleTerm Gold serial program in Windows with Hex, Ascii, etc.
GNU C compiler in Linux for offline analysis
ExpressPCB Layout Software
Eagle PCB Layout Software

Data collection

Data collection for a system of significant size is envisioned as a three step process. We can consider total bandwidth at each stage, and both with and without de-randomization at the later stages.
We also consider cost.

First the bits from the parallel shift registers are shifted to microcontrollers on the edge of the RPC plane.

Secondly, data is sent in bytes to an intermediate collector, either one or two per calorimeter plane. An identification word from each microcontroller can be added during this stage. This process could use the tri-state outputs of the microcontrollers.
De-randomizing buffer memory at this stage would reduce dead time significantly.
This would require event numbers and/or token numbers to be added to the data at this stage.

Thirdly, the data from many intermediate collectors can be sent at much higher rate to a single channel which would go to a PC. The data path to the PC could be VME or USB, etc. Rates and Bandwidth are discussed below.

We describe two scales, systems for RPCs of 50x50 pads x 40 layers, and 100x100 pads with 40 layers. The diagrams are for the 100x100 system.

For a 50x50x40 RPC, (100K pads) and 1000 u sec readout time at the first stage, the peak bandwidth with no de-randomization would be around 16 M Byte/sec. With an average trigger rate of 100Hz, and derandomizing buffers, this would be down to 1.6 MB/sec to a PC.
This is easily handled by technologies such as USB2 or VME.

We give some explicit numbers for a 50x50 x40 system. For 50 pads in a row, and the 74hc165 chip reading both sides, there are 26 rows of 13 chips.
With the measured input rate of almost 5 u sec/bit + overhead, it would take about 500 u sec to read parallel strings of 104 bits (two columns of 50 pads, + end effects) for 26 u controllers.
There are 338 bytes of data per plane. This could be put out as 26 bytes from each u controller in less than 20 u sec from each u controller if 8 bit wide. If these were dumped one after the other to a single input to a collector, it would take 500 u sec to read a plane to an intermediate collector.

From the point of view of the overall system, the RPC itself can't take rates more than 1 kHz in a small area (1 milli sec), and one would limit the beam rate to something like 100 Hz.

Prototyping Data collection for tests of up to 100 channels should be straightforward as it was for 32. A single microcontroller can read out a dozen or so cascaded parallel to serial shift registers. The data for an event can be buffered on the microcontroller.
The data can be sent by RS232 to a PC.

For small tests, data can be sent by serial to a PC. This could all be done once per event, with some dead time. The slowest part would be RS232 to the PC if it were done this way.

For more serious data collection, the microcontrollers have 8 bit tri-state outputs and flow control.Microcontrollers with enough pins for parallel output are available.

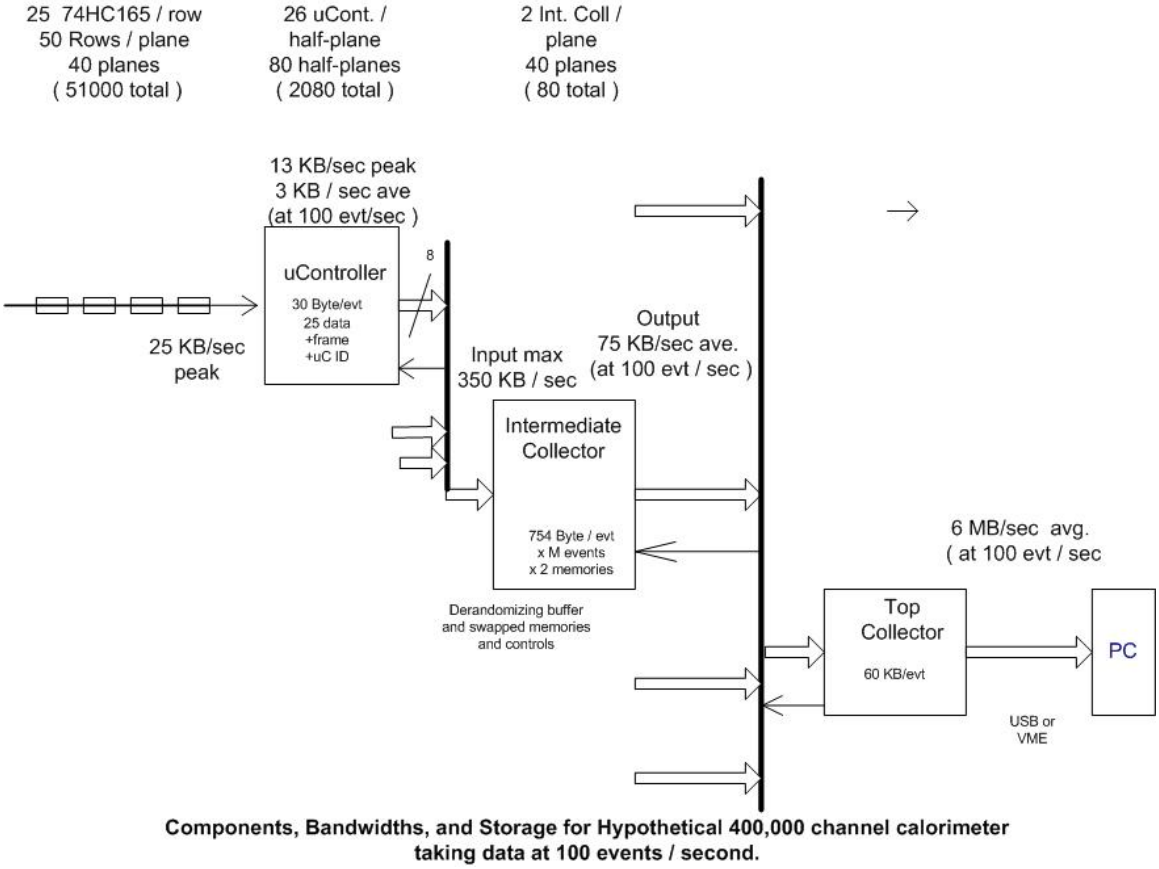


Fig. 11 Organization of a full-scale data collection system for a calorimeter of 400K channels.

Cost Scaling

One issue here is start-up costs for various approaches vs ultimate cost and ultimate functionality. Another issue is the time scale for having a multi-layer calorimeter for a test.

We could design a system for immediate use in scaled down detectors for electron beam or cosmic ray tests of eg a 24 cm x 24 cm x 40 layer system of 25 K channels. It would have a vastly smaller start-up costs than an ASIC version.

Component vs ASIC						
	cost ea	number	tot cost	number	tot cost	Reference
		400k chan	400k chan	30k chan	30k chan	
PC boards						
ASIC 9 layer	250	360	90000	50		funding me
Component 4 layer	166	360	60000	50	7500	
Board Assembly						
ASIC			1500			
Component			73000		10400	Co. Z
Parts						
ASIC	29	6250	181250	480	13920	
Component			94173		7190	
lm3900	0.39	104000	40560	7500	2925	
74hc165	0.11	58300	6413	7500	825	
ts3704	0.3	104000	31200	7500	2250	
capacitor	0.05	200000	10000	15000	750	
resistor	0.02	300000	6000	22000	440	
Total						
ASIC			272750			
Component			227173			

Fig 12 Cost comparison for stuffed boards, not including readout or contingency.

Additional parts of rough cost estimate including only first stage of reading, not the full DAQ:
In addition to above spreadsheet for boards:
PIC16F87 Microcontroller (1 per 64 chan)
6$ / 64 with socket -> 0.20/ch
(This is part of the readout system)
Power supplies $1500 / 25K chan -> 0.06/ch
Programmable DAC, etc for threshold $10 /600 ch -> 0.02/ch

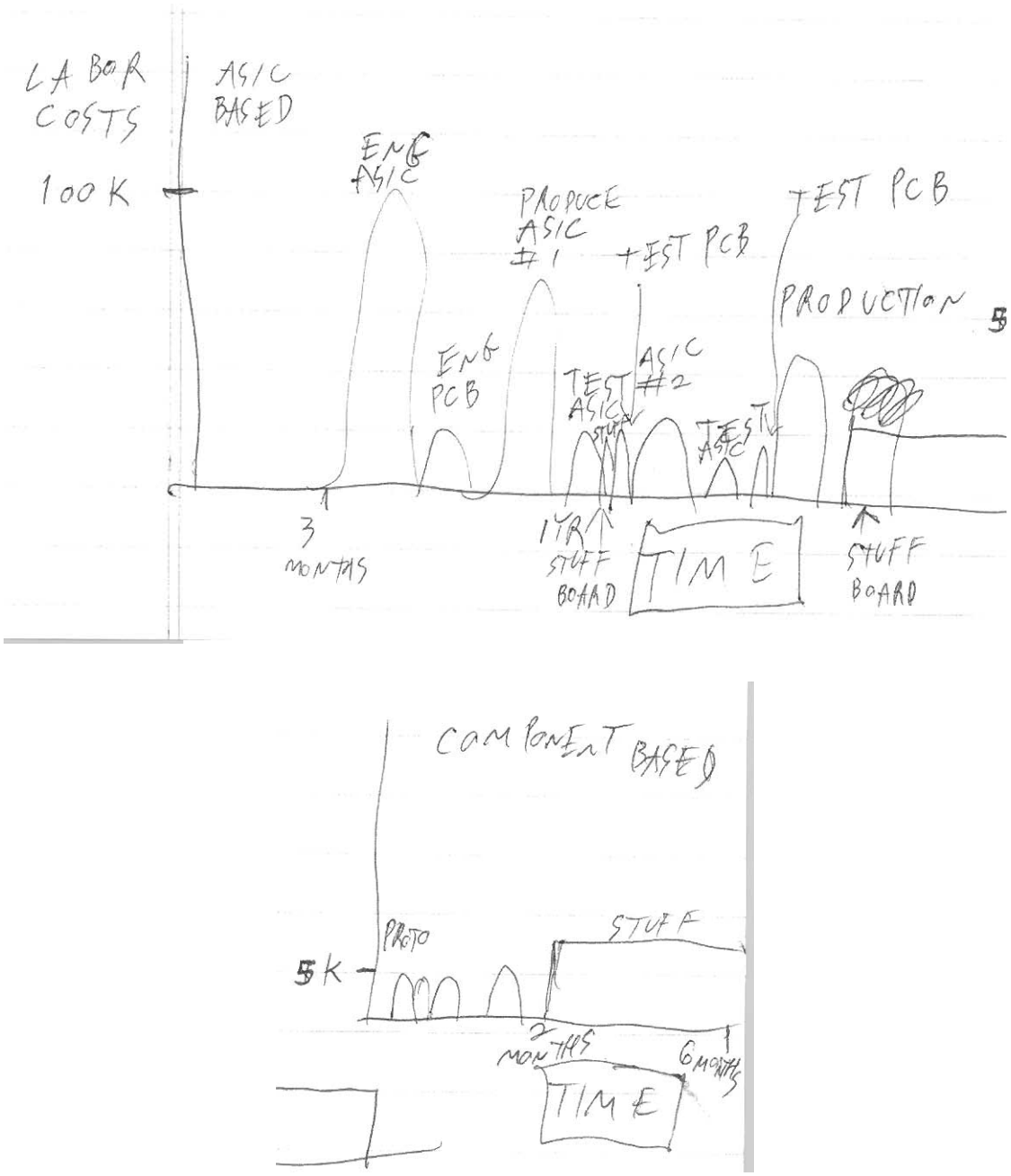


Fig 13 Sketches of spending profiles for two approaches.

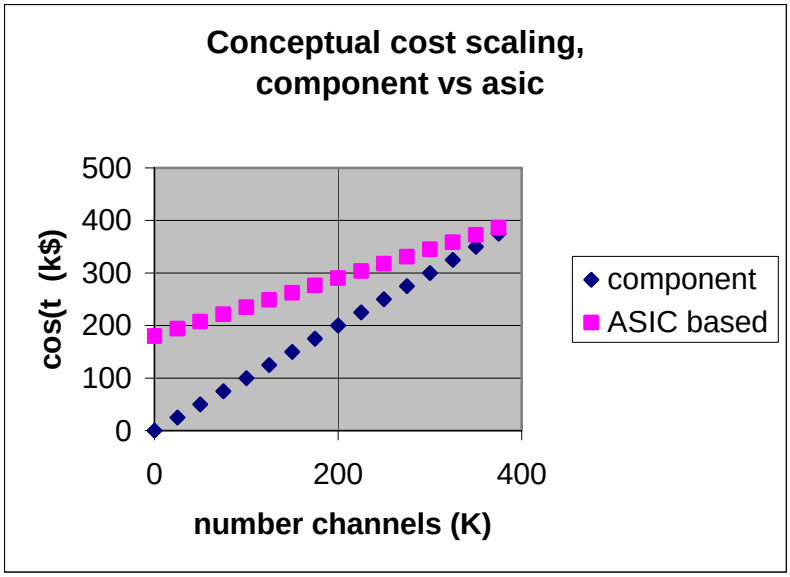


Fig 14 A conceptual cost scaling, comparing a project which is front-loaded with development costs in order to produce low cost per unit for large quantities VS one which has small development costs but higher costs for assembly at each stage.

Besides there being an existence proof that the shift register can be done on some scale, and the low startup costs and similar overall costs, what other advantages might this method have?

1) Hardware addresses can be inserted for each row of readout on a plane, and put into the data at an early stage, in the microcontroller near the RPC. This should allow easier debugging, and fewer mistakes.

2) How many signals need to be jumpered where readout boards are mated edge to edge? (A square meter is probably covered by 3 x 3 or 9 PC boards because the PC boards cannot be made any larger in an economical way.) For the shift register, there are clock, load, data 5V, 8 V and 1 or 2 grounds for each pair of pad rows (24- 30 lines / 8 pad rows) And most of these are on the top surface in the present implementation.

What are the signals for the ASIC? How wide is the bus out of the chip? N lines / 8 pad rows? How many of these have to be brought to the surface from buried layers?

3) The tree structure of the shift-register daq / readout is done in a different way than that proposed for an ASIC. The first stage is done with commercial microcontroller chips at low cost per channel. The last stage might avoid the cost of VME cards and crates, depending on the cost of engineering cost involved to do a USB readout, compatibility with other parts of an experiment, etc.

4) It scales to a system of eg ¼ as many channels, with a much smaller cost penalty due to overhead. This allows small tests with eg electron test beams, a few layers in a hadron beam, etc.

APPENDIX A : REQUIREMENTS

(rates, gate widths, charge sensitivity, non-linearity, readout times, etc)

Rates:

Beamline:

We would like to accumulate at least 1000 hadronic events and 100 electromagnetic events at two energies in 5 days of test beam run. 5 days is 4 x 10^5 seconds Assume 25% of the accelerator cycle time is slow spill time. Assume the accelerator and beamline, etc operate 50% of the time. Assume the experiment debugs for half the beam time, and then has 50% efficiency after that. This leaves 6000 seconds for each energy. So 1 event per second is more than adequate. How low can beam intensities be turned down?

Cosmics:

The cosmic flux through a square meter is less than 300/sec.
A single readout-pad is about 10^-4 meter^2, so 1 per sec would be adequate for each amplifier if there were no anomalously noisy RPC chambers.
The digital readout will have to operate at the trigger rate. We have only crude ways based on multiplicity in scintillator arrays to select hadrons in cosmic rays, so assume a trigger on every cosmic within our area and solid angle. This could be around 20/sec..

Internal noise:

In the literature one finds claims of 1 KHz/m^2. A single readout-pad is about 10^-4 meter^2, so again, 1 per sec would be adequate for each amplifier if there were no anomalously noisy RPC chambers.

Gate widths.

RPC's (and most detectors) have background noise rates. A long acceptance gate or long integration time will collect these along with the signal. With the slow amplifiers proposed here, the rise time to the discriminator threshold can range from fractions of a micro-second to a few micro-seconds. With a gate of 10 microseconds, and a noise rate of 1 KHz/plane, and 40 planes, the average number of noise hits would be less than 1 per event. (1 pad out of 400 K pads) With 300 cosmics per second, 0.3% of all events (from any source – cosmics, beam, etc) would contain a cosmic ray

(non)-linearity:

There is no particular advantage in having a linear system if we only want a yes-no answer at the end. In fact, for large signals it is good if the amplifiers saturate in a controlled way which does not create excess dead time. We do need to be able to set the gain so that the threshold can be adjusted for good efficiency and is similar from one pad to another. With the proposed (and tested) amplifier chips, the output saturates at about

100 mv for all real signals, with the amplifier in a different mode of operation for very large breakdown signals. It is found experimentally that a threshold of 30 mv gives the efficiency corresponding to a 60 fC threshold when the amplifiers are operated at 8.6 volts.

Masking bad channels:

Since there is no self-trigger, bad channels will simply be read in with all channels. They can be suppressed offline if desired. No on-line mask is needed.

Dead Time:

This system has dead time. This is a price for using a very simple system with off-the shelf-components. If the readin capability is Nx100 Hz, and the trigger rate is Nx10 Hz, then there would be roughly 10% dead time. At rates which give more than 50% dead time, events are very close in time for some fraction of the events. We should probably avoid this. (This time is still not near the 20 microsecond amplifier recovery time or the 1 milli-second RPC recovery time for small areas.)

Appendix C: Hadrons in cosmic Rays

What could be done with high energy protons in cosmic rays? The fraction of cosmic rays at the earth's surface that are protons is around 10^-2 at 1 GeV and around 10^-3 between 3 and 6 GeV.
http://www.research.ibm.com/journal/rd/421/zeigler.html
This gives a couple per hour for a small calorimeter looking at cosmics. In our cosmic ray test stand at Argonne, we collect about 2 million cosmics per week. This would be a few hundred hadronic events per week.
We can find these by a combination of multiplicity in the trigger and tagging counters, and multiplicity in the digital calorimeter.
We will not have an a-priori momentum measurement, but the high multiplicity of tracks in a real digital calorimeter should be invaluable for tuning software.

What can be learned with EM showers only or with EM showers plus the core of hadronic? We can make a calorimeter 24 cm by 24 cm by 40 layers with about 1/16 the number of channels of a cubic meter. (or 32 x 32 with 10% of the channels, etc) This could be used for studies and software development while awaiting the full system.

APPENDIX C: LM3900 Amplifier

All the early tests of the LM3900 for use with RPC signals were with the circuit A. The gain of this circuit is sensitive to small differences between similar currents. These currents were set by using small differences, typically 20K ohms, between resistors which were approximately 1 meg-ohm. The later circuit B does not have the problems of using differences between currents, and is also vastly less sensitive to variation between channels in a chip.

DC Voltage out response to current in is S-shaped, low for neg, big slope at 0, close to sat for a range of big + currents. For Amplifier A we bias it below 0 where slope is as sensitive as possible while maintaining stability. For amplifier B we can bias it for maximum sensitivity (output voltage is mid-range).

Tests using Amplifier circuit A:

For DC bias we put slightly less + current into the + input, this drives output more – than with no bias. DC bias we put slightly more + current into the – input. This drives output more – than with no bias. Signal is – into – input, which drives output +.

Neg signal into neg input drives it +. Hypothesis is that we get 100 mv instead of 5 v signal because it saturates in the front end with 1 uA signal, and we only get 100 mV because of frequency response with 1 MHz low pass filter built in.

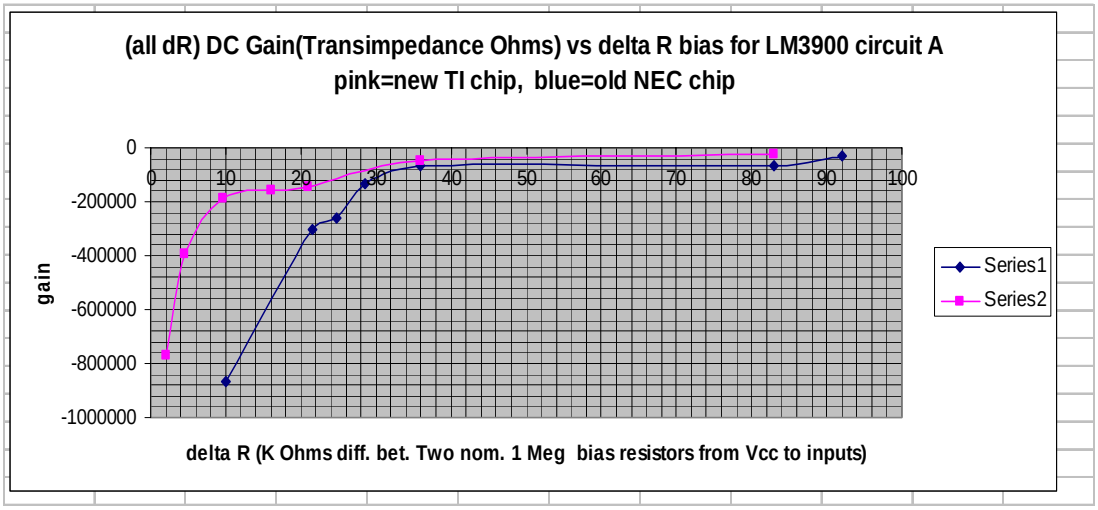


Fig 15 DC gain measurements for two versions of the LM3900 Amplifier chip vs the bias. dR is the difference in resistance between resistors to the + and – inputs which are approximate 1 Meg Ohm each. Gain was measured as difference in output voltage Vs difference in input current.

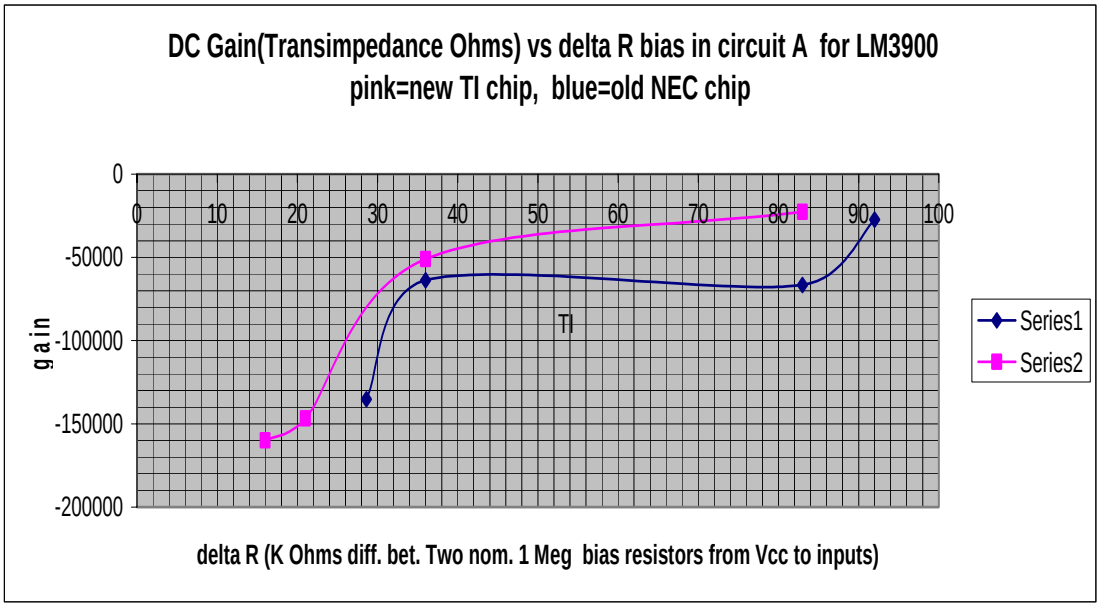


Fig. 16 DC gain measurements on an expanded scale in the region of actual operation.

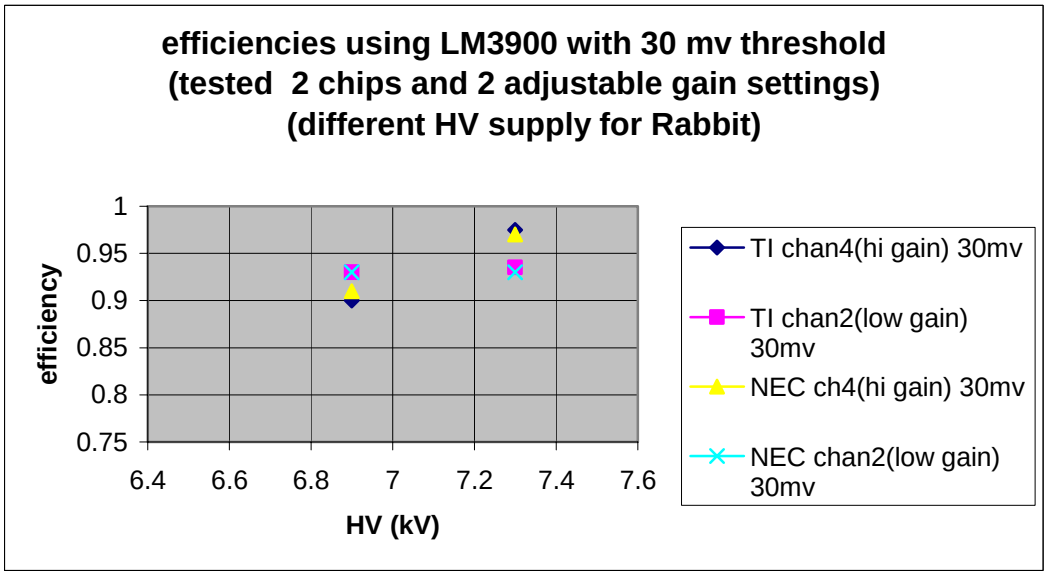


Fig. 17 Efficiencies with low and high gain bias of LM3900 using circuit A. Low gain is with a bias current difference of 300 nA and high gain is with a bias current of 100 nA.

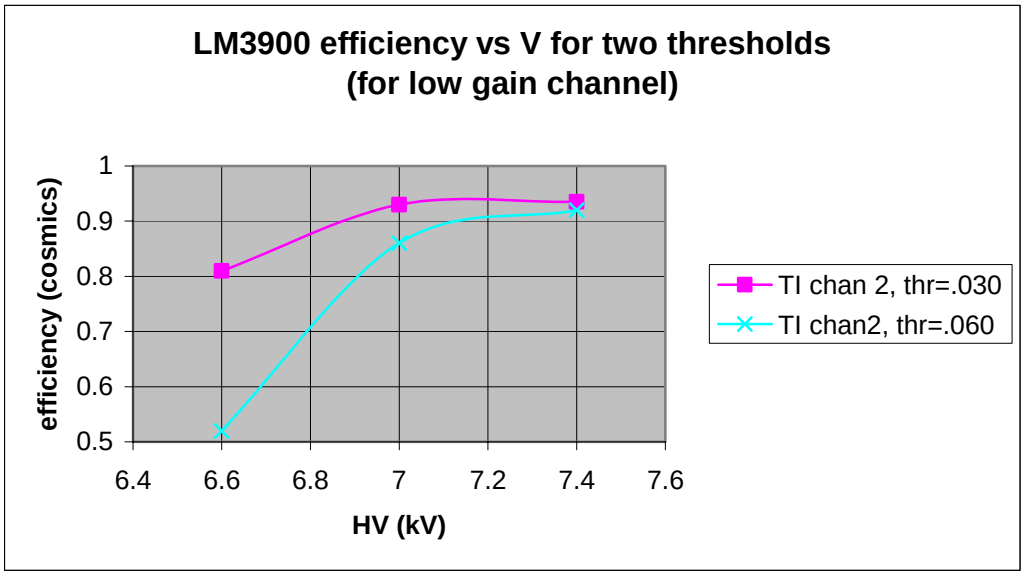


Fig. 18 Efficiency vs two different Discriminator thresholds for a channel of amplifier circuit A. This was deliberately done with non-optimal biasing, because we expected problems with channel-to-channel variation using circuit A.

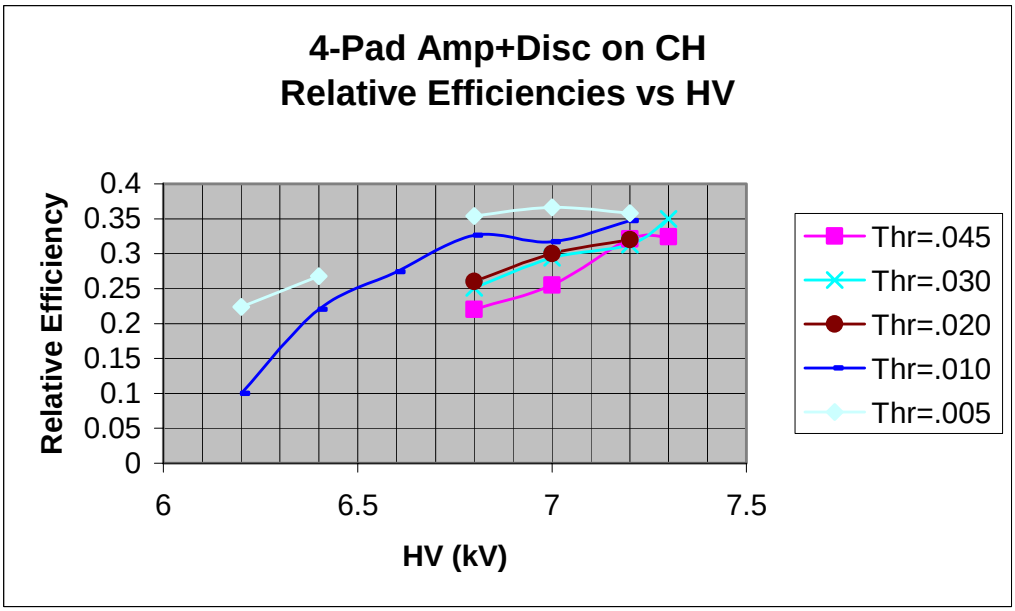


Fig. 19 Relative efficiency (with amplifier A) measured for various thresholds and RPC high Voltage with 4 pads of 1 cm^2, and a beta source.